Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Withdrawn) A bonding pad structure disposed on a surface of a semiconductor substrate with a circuit therein, comprising:

a bottom metal layer disposed over the surface of the semiconductor substrate to connect the circuit electrically;

an inter-metal dielectric layer disposed over the bottom metal layer;

a plurality of metal plugs formed therein the inter-metal dielectric layer to connect with the bottom metal layer;

a top metal layer disposed over the inter-metal dielectric layer connecting with the metal plugs; and

a passivation layer disposed over the top metal layer with a plurality of openings to expose the top metal layer portions as bonding pads, wherein at least one bonding pad is mark-shaped to indicate the orientation of the bonding pads on the semiconductor substrate.

2. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the mark shaped bonding pad is a "凸" shape.

3. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the mark-shaped bonding pad is a "凹" shape.

4. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the mark-shaped bonding pad is a cross shape "✚".

5. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the mark-shaped bonding pad is a " ⌜" shape.

6. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the top and bottom metal layers are an alloy of aluminum and copper or an alloy of aluminum, copper and silica.

7. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the inter-metal dielectric layer is a silicon oxide.

8. (Withdrawn) The bonding pad structure as claimed in claim 1, wherein the passivation layer is silicon oxide or borophosphosilicate glass and silicon nitride.

9. (Currently Amended) A probe pad on a semiconductor circuit for electric characteristic measurement, wherein an exposed portion of the probe pad ~~comprising~~ has a mark-shape contour to indicate the relative location of the probe pad on the semiconductor circuit.

10. (Previously Presented) The probe pad as claimed in claim 9, wherein the mark-shaped contour is a shape showing relative positions with each other.

11. (Previously Presented) The probe pad as claimed in claim 10, wherein the mark-shaped contour is a "⏃" ,"✚" or " ⌜" shape.

12. (Canceled)

13. (Canceled)

14. (Original) The probe pad as claimed in claim 9, wherein the probe pad is an alloy of aluminum and copper or an alloy of aluminum, copper and silica.

15. (Withdrawn) A method for forming a bonding pad structure on a surface of a semiconductor substrate with a circuit therein, comprising:

disposing a bottom metal layer over the surface of the semiconductor substrate to connect the circuit electrically;

disposing an inter-metal dielectric layer over the bottom metal layer;

forming a plurality of metal plugs in the inter-metal dielectric layer to connect with the bottom metal layer;

disposing a top metal layer over the inter-metal dielectric layer to connect with the metal plugs;

disposing a passivation layer over the top metal layer; and

defining a plurality of openings on the passivation layer to expose the top metal layer portions as bonding pads,

wherein at least one bonding pad is defined as a mark-shape to indicate the orientation of the bonding pads on the semiconductor substrate.

16. (Withdrawn) The method as claimed as in claim 15, wherein the mark-shaped bonding pad is defined as a "凸" shape.

17. (Withdrawn) The method as claimed as in claim 15, wherein the mark-shaped bonding pad is defined as a "凹" shape.

18. (Withdrawn) The method as claimed as in claim 15, wherein the mark-shaped bonding pad is defined as a cross shape "✚".

19. (Withdrawn) The method as claimed as in claim 15, wherein the mark-shaped bonding pad is defined as a " ⊩" shape.

20. (New) A probe pad on a semiconductor circuit for electric characteristic measurement, wherein an entirety of the probe pad has a mark-shape contour to indicate the relative location of the probe pad on the semiconductor circuit.

21. (New) The probe pad as claimed in claim 20, wherein the mark-shaped contour is a shape showing relative positions with each other.

22. (New) The probe pad as claimed in claim 21, wherein the mark-shaped contour is a "凸", "✚" or " ⊩"shape.